I claim:

1. A fuse circuit, comprising:

a volatile latch; and

a nonvolatile fuse adapted to operate with a voltage supply greater than about 1.65 volts, wherein the voltage supply is boosted at a desired time to a predetermined level and for a predetermined duration so that the nonvolatile fuse transfers its data to the volatile latch.

2. The fuse circuit of claim 1, wherein the nonvolatile fuse includes a flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts.

3. The fuse circuit of claim 1, wherein the volatile latch includes a pair of inverters.

4. The fuse circuit of claim 1, wherein the nonvolatile fuse refrains from transferring its data when the nonvolatile fuse is in a programmed state.

5. The fuse circuit of claim 1, wherein the nonvolatile fuse transfers its data when the nonvolatile fuse is in an erased state.

6. A fuse circuit, comprising:

an input stage produces a gating signal; and

a nonvolatile fuse having a first, a second, and a third connection, wherein the first connection receives the gating signal, and wherein the gating signal is boosted so that the nonvolatile fuse selectively transfers its data.

7. The fuse circuit of claim 6, wherein the input stage includes a transistor having a gate, a drain, and a source, wherein the gate receives a voltage supply that is greater than about 1.65 volts, wherein the drain receives an enabling signal, and wherein the source presents the gating signal.

8. The fuse circuit of claim 7, wherein the input stage includes an inverter having a first and a second connection, wherein the first connection of the inverter receives the enabling signal, and wherein the second connection presents a gating signal.

9. The fuse circuit of claim 6, wherein the nonvolatile fuse includes a threshold voltage, wherein the gating signal, which is boosted to a level greater than the threshold voltage, turns on the nonvolatile fuse if the nonvolatile fuse is in an erased state.

10. The fuse circuit of claim 6, wherein the nonvolatile fuse is a flash cell.

11. A fuse circuit, comprising:

an input stage that presents a gating signal;

a boosting stage that produces a boosting signal; and

a nonvolatile fuse having a first, a second, and a third connection, wherein the first connection receives the gating signal, and wherein the gating signal is boosted by the boosting stage so that the nonvolatile fuse selectively transfers its data.

12. The fuse circuit of claim 11, wherein the boosting stage includes an energy-storing device having a first connection and a second connection, wherein the second connection of the energy-storing device receives the gating signal.

13. The fuse circuit of claim 12, wherein the boosting stage includes an inverter having a first and a second connection, wherein the first connection of the boosting stage receives a transferring signal, and wherein the second connection presents the boosting signal to the first connection of the energy-storing device.

14. The fuse circuit of claim 13, wherein the energy-storing device stores a first level of energy when the boosting signal is low and the gating signal is high.

15. The fuse circuit of claim 14, wherein the energy-storing device boosts the first level of energy to the second level of energy when the boosting signal is high and the gating signal is high.

16. A fuse circuit, comprising:

an input stage that presents a gating signal;

a boosting stage that produces a boosting signal;

a transfer stage receptive to a transferring signal; and

a nonvolatile fuse having a first, a second, and a third connection, wherein the first connection receives the gating signal, and wherein the gating signal is boosted by the boosting stage so that the transfer stage transfers the data of the nonvolatile fuse.

17. The fuse circuit of claim 16, wherein the transfer stage includes an inverter having a first and a second connection, wherein the first connection is receptive to a transferring signal, and wherein the second connection presents a switching signal.

18. The fuse circuit of claim 17, wherein the transferring stage includes a p-channel transistor having a gate, a drain, and a source, wherein the gate receives the switching signal, wherein the drain receives a voltage supply that is greater than

about 1.65 volts.

19. The fuse circuit of claim 18, wherein the transferring stage includes an n-channel transistor having a gate, a drain, and a source, wherein the gate of the n-channel transistor receives the switching signal, wherein the drain of the n-channel transistor couples to the source of the p-channel transistor, wherein the source of the n-channel transistor couples to the second connection of the nonvolatile fuse.

20. The fuse circuit of claim 19, wherein the nonvolatile fuse includes a flash cell having a gate, a drain, and a source, wherein the gate of the flash cell couples to the boosting stage, wherein the drain of the flash cell couples to the source of the n-channel transistor, and wherein the source of the flash cell couples to ground.

21. A fuse circuit, comprising:

an input stage that presents a gating signal;

a boosting stage that produces a boosting signal;

a transfer stage receptive to a transferring signal;

a latch receptive to data that is transferred by the transfer stage; and

a nonvolatile fuse that includes a flash cell having a gate, a drain, and a source, wherein the gate receives the gating signal, wherein the drain couples to the transfer stage, and wherein the source couples to ground.

22. The fuse circuit of claim 21, wherein the input stage receives an enabling signal and presents the gating signal.

23. The fuse circuit of claim 22, wherein the boosting stage receives the gating signal and stores a first level of energy, and wherein the boosting stage boosts the first level of energy to a second level of energy when the boosting signal is high.

24. The fuse circuit of claim 23, wherein the transfer stage switches the latch to a voltage supply that is greater than about 1.65 volts when the transferring signal is high, and wherein the transfer stage switches the latch to the flash cell when the transferring signal is low.

25. The fuse circuit of claim 24, wherein the flash cell transfers its data to the transfer stage for transferring to the latch when the flash cell receives the second level of energy from the boosting stage at a level that is greater than a threshold voltage.

26. A method for enhancing a fuse circuit in a low-voltage IC, comprising:

presenting by an input stage a gating signal;

boosting by a boosting stage the gating signal; and

transferring selectively by a nonvolatile fuse having a first, a second, and a third connection, wherein the first connection receives the gating signal that is boosted so that the nonvolatile fuse selectively transfers its data.

27. The method of claim 26, wherein boosting includes storing by an energy-storing device having a first connection and a second connection, wherein the second connection of the energy-storing device receives the gating signal.

28. The method of claim 27, wherein boosting includes inverting by an inverter having a first and a second connection, wherein the first connection of the boosting stage receives a transferring signal, and wherein the second connection presents the boosting signal to the first connection of the energy-storing device.

29. The method of claim 28, wherein storing includes storing a first level of energy when the boosting signal is low and the gating signal is high.

30. The method of claim 29, wherein boosting includes boosting the first level of energy to the second level of energy when the boosting signal is high and the gating signal is high.

31. A method for enhancing a fuse circuit in a low-voltage IC, comprising:

presenting by an input stage a gating signal;

boosting by a boosting stage the gating signal;

transferring by a transfer stage a data; and

providing the data to the transfer stage by a nonvolatile fuse having a first, a second, and a third connection, wherein the first connection receives the gating signal that is boosted..

32. The method of claim 31, wherein transferring includes inverting by an inverter having a first and a second connection, wherein the first connection is receptive to a transferring signal, and wherein the second connection presents a switching signal.

33. The method of claim 32, wherein transferring includes switching by a p-channel transistor having a gate, a drain, and a source, wherein the gate receives the switching signal, wherein the drain receives a voltage supply that is greater than about 1.65 volts.

34. The method of claim 33, wherein transferring includes switching by an n-channel transistor having a gate, a drain, and a source, wherein the gate of the n-channel transistor receives the switching signal, wherein the drain of the n-channel transistor couples to the source of the p-channel transistor, wherein the source of the n-channel transistor couples to the second connection of the nonvolatile fuse.

35. The method of claim 34, wherein providing includes providing by a flash cell having a gate, a drain, and a source, wherein the gate of the flash cell couples to the boosting stage, wherein the drain of the flash cell couples to the source of the n-channel transistor, and wherein the source of the flash cell couples to ground.

36. A method for enhancing a fuse circuit in a low-voltage IC, comprising:

presenting by an input stage a gating signal;

boosting by a boosting stage the gating signal;

transferring by a transfer stage a data;

latching by a latch the data transferred by the transfer stage; and

providing the data by a nonvolatile fuse that includes a flash cell having a gate, a drain, and a source, wherein the gate receives the gating signal, wherein the drain couples to the transfer stage, and wherein the source couples to ground.

37. The method of claim 36, further comprising receiving an enabling signal by the input stage, and wherein the act of receiving the enabling signal precedes the act of presenting the gating signal.

38. The method of claim 37, wherein boosting includes receiving the gating signal and storing a first level of energy, and wherein the act of boosting boosts the first level of energy to a second level of energy when a boosting signal, which is produced by the boosting stage, is high.

39. The method of claim 38, wherein transferring includes coupling the latch to a voltage supply that is greater than about 1.65 volts when a transferring signal, which is presented to the transfer stage, is high, and wherein transferring includes coupling the latch to the flash cell when the transferring signal is low.

40. The method of claim 39, wherein providing includes providing by the flash cell its data to the transfer stage for transferring to the latch when the flash cell receives the second level of energy from the boosting stage at a level that is greater than a threshold voltage.

41. A fuse bank in a low-voltage integrated circuit, comprising:

a fuse circuit, including:

an input stage that presents an inverted enabling signal;

a boosting stage that produces a boosting signal;

a transfer stage receptive to a transferring signal;

a latch receptive to data that is transferred by the transfer stage;

a nonvolatile fuse that includes a flash cell having a gate, a drain, and a source, wherein the gate receives the gating signal, wherein the drain couples to the transfer stage, and wherein the source couples to ground;

a matching circuit receptive to the data from the latch to produce a matching signal; and

a fuse disabling circuit to disable the fuse circuit if the fuse circuit is impaired.

42. A wireless device, comprising:

a display;

a processor; and

a flash memory device that includes a redundancy circuit having a fuse circuit, the fuse circuit includes:

an input stage that presents a gating signal;

a boosting stage that produces a boosting signal;

a transfer stage receptive to a transferring signal;

a latch receptive to data that is transferred by the transfer stage; and

a nonvolatile fuse that includes a flash cell having a gate, a drain, and a source, wherein the gate receives the gating signal, wherein the drain couples to the transfer stage, and wherein the source couples to ground.

43. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

an input stage to present a gating signal;

a boosting stage to boost the gating signal;

a transferring stage coupled to receive a transferring signal;

a latch coupled to receive data to be transferred by the transferring stage; and

a flash cell to hold the data, the flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain coupled to the transferring stage, and a source coupled to ground;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

44. The fuse bank of claim 43 wherein:

the integrated circuit comprises a flash memory device;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises a p-channel transistor coupled between a voltage supply in the range of 1.65 volts to 2.22 volts and the latch, and an n-channel transistor coupled between the latch and the drain of the flash cell, a gate of the p-channel transistor being coupled to a gate of the n-channel transistor to receive the transferring signal, the p-channel transistor to couple the latch to the voltage supply in response to a low transferring signal and the n-channel transistor to couple the latch to the drain of the flash cell to transfer the data in response to a high transferring signal;

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a first

level of energy based on the voltage supply to a second level of energy in response to a high boosting signal;

the latch comprises an output of a first inverter coupled to an input of a second inverter and the transferring stage and an output of the second inverter coupled to an input of the first inverter; and

the flash cell is enabled to transfer the data to the transferring stage and the latch when the gating signal is at the second level of energy, the flash cell being turned on by the second level of energy if the flash cell is erased and the flash cell not being turned on by the second level of energy if the flash cell is programmed.

45. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

a volatile latch circuit to latch data;

a nonvolatile fuse to hold the data; and

a boost circuit to boost a gating signal on the nonvolatile fuse to enable the nonvolatile fuse to transfer the data;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

46. The fuse bank of claim 45 wherein:

the integrated circuit comprises a flash memory device;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being boosted from a voltage supply in the range of 1.65 volts to 2.22 volts, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter;

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell in response to the boosting signal.

47. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

a volatile latch circuit to latch data;

a flash cell to hold the data; and

a boost circuit to boost a gating signal on the flash cell to enable the flash cell to transfer the data;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

48. The fuse bank of claim 47 wherein:

the integrated circuit comprises a flash memory device;

the flash cell comprises a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter; and

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a voltage

supply in the range of 1.65 volts to 2.22 volts in response to the boosting signal.

49. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

a volatile latch; and

a nonvolatile fuse to hold data, the nonvolatile fuse being adapted to operate with a voltage supply greater than about 1.65 volts, the voltage supply to be boosted to a predetermined level for a predetermined duration to enable the nonvolatile fuse to transfer the data to the volatile latch;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

50. The fuse bank of claim 49 wherein:

the integrated circuit comprises a flash memory device;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and an output of the second inverter coupled to an input of the first inverter;

the nonvolatile fuse comprises a flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the voltage supply comprises a voltage supply in the range of 1.65 volts to 2.22 volts;

the voltage supply is to be boosted to about double the voltage supply by a boost circuit comprising a capacitor coupled to a gate of the flash cell; and

the boosted voltage is sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted voltage is insufficient to turn on the flash cell if the flash cell is in a programmed state.

51. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

an input stage to produce a gating signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

52. The fuse bank of claim 51 wherein:

the integrated circuit comprises a flash memory device;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the input stage comprises:

a transistor comprising a gate, a drain, and a source, the gate of the transistor being coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, the drain of the transistor being coupled to receive an enabling signal, and the source of the transistor being coupled to the gate of the flash cell to present the gating signal; and

an inverter having an input coupled to receive the enabling signal and an output coupled to the transistor; and

the boosted gating signal is to be boosted from the voltage supply, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state.

53. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

54. The fuse bank of claim 53 wherein:

the integrated circuit comprises a flash memory device;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the boosting stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate the boosting signal;

a capacitor having a first connection coupled to the output of the inverter to receive the boosting signal and a second connection coupled to the gate of the flash cell

to boost the gating signal, the capacitor to store a first level of energy based on a voltage supply in the range of 1.65 volts to 2.22 volts when the boosting signal is low and the gating signal is high and to boost the first level of energy to a second level of energy when the boosting signal is high and the gating signal is high.

55. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal;

a transferring stage coupled to receive a transferring signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage and the boosting stage to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to transfer the data to the transferring stage;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

56. The fuse bank of claim 55 wherein:

the integrated circuit comprises a flash memory device;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling

signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate a switching signal in response to the transferring signal;

a p-channel transistor having a gate coupled to receive the switching signal, a source coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, and a drain; and

an n-channel transistor having a gate coupled to receive the switching signal, a drain coupled to the drain of the p-channel transistor, and a source coupled to the drain of the flash cell; and

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from the voltage supply in response to the boosting signal.

57. A fuse bank in an integrated circuit comprising:

a fuse circuit in an integrated circuit comprising:

a volatile latch;

a nonvolatile fuse; and

means for transferring data from the nonvolatile fuse to the volatile latch;

a match circuit in the integrated circuit coupled to receive the data from the latch to produce a match signal in response to the data; and

a disable circuit in the integrated circuit to disable the fuse circuit if the fuse circuit is unreliable.

58. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch; and

a nonvolatile fuse to hold data, the nonvolatile fuse being adapted to operate with a voltage supply greater than about 1.65 volts, the voltage supply to be boosted to a predetermined level for a predetermined duration to enable the nonvolatile fuse to transfer the data to the volatile latch.

59. The wireless device of claim 58 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and an output of the second inverter coupled to an input of the first inverter;

the nonvolatile fuse comprises a flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the voltage supply comprises a voltage supply in the range of 1.65 volts to 2.22 volts;

the voltage supply is to be boosted to about double the voltage supply by a boost circuit comprising a capacitor coupled to a gate of the flash cell; and

the boosted voltage is sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted voltage is insufficient to turn on the flash cell if the flash cell is in a programmed state.

60. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to produce a gating signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data.

61. The wireless device of claim 60 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the flash cell having a threshold voltage of greater than about 2.5 volts and less than about 3.5 volts;

the input stage comprises:

a transistor comprising a gate, a drain, and a source, the gate of the transistor being coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, the drain of the transistor being coupled to receive an enabling signal, and the source of the transistor being coupled to the gate of the flash cell to present the gating signal; and

an inverter having an input coupled to receive the enabling signal and an output coupled to the transistor; and

the boosted gating signal is to be boosted from the voltage supply, the boosted

gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state.

62. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to selectively transfer the data.

63. The wireless device of claim 62 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a

programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the boosting stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate the boosting signal;

a capacitor having a first connection coupled to the output of the inverter to receive the boosting signal and a second connection coupled to the gate of the flash cell to boost the gating signal, the capacitor to store a first level of energy based on a voltage supply in the range of 1.65 volts to 2.22 volts when the boosting signal is low and the gating signal is high and to boost the first level of energy to a second level of energy when the boosting signal is high and the gating signal is high.

64. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage coupled to the input stage to boost the gating signal in response to a boosting signal;

a transferring stage coupled to receive a transferring signal; and

a nonvolatile fuse to hold data, the nonvolatile fuse having a first connection coupled to the input stage and the boosting stage to receive the gating signal, a second connection, and a third connection, the gating signal to be boosted to enable the nonvolatile fuse to transfer the data to the transferring stage.

65. The wireless device of claim 64 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises:

an inverter having an input coupled to receive a transferring signal and an output to generate a switching signal in response to the transferring signal;

a p-channel transistor having a gate coupled to receive the switching signal, a source coupled to receive a voltage supply in the range of 1.65 volts to 2.22 volts, and a drain; and

an n-channel transistor having a gate coupled to receive the switching signal, a drain coupled to the drain of the p-channel transistor, and a source coupled to the drain of the flash cell; and

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from the voltage supply in response to the boosting signal.

66. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

an input stage to present a gating signal;

a boosting stage to boost the gating signal;

a transferring stage coupled to receive a transferring signal;

a latch coupled to receive data to be transferred by the transferring stage; and

a flash cell to hold the data, the flash cell comprising a gate coupled to the input stage to receive the gating signal, a drain coupled to the transferring stage, and a source coupled to ground.

67. The wireless device of claim 66 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the input stage comprises an inverter coupled in series with a transistor that is coupled to the gate of the flash cell, the inverter being coupled to receive an enabling signal, the transistor to generate the gating signal in response to the enabling signal;

the transferring stage comprises a p-channel transistor coupled between a voltage supply in the range of 1.65 volts to 2.22 volts and the latch, and an n-channel transistor coupled between the latch and the drain of the flash cell, a gate of the p-channel transistor being coupled to a gate of the n-channel transistor to receive the transferring signal, the p-

channel transistor to couple the latch to the voltage supply in response to a low transferring signal and the n-channel transistor to couple the latch to the drain of the flash cell to transfer the data in response to a high transferring signal;

the boosting stage comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a first level of energy based on the voltage supply to a second level of energy in response to a high boosting signal;

the latch comprises an output of a first inverter coupled to an input of a second inverter and the transferring stage and an output of the second inverter coupled to an input of the first inverter; and

the flash cell is enabled to transfer the data to the transferring stage and the latch when the gating signal is at the second level of energy, the flash cell being turned on by the second level of energy if the flash cell is erased and the flash cell not being turned on by the second level of energy if the flash cell is programmed.

68. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch circuit to latch data;

a nonvolatile fuse to hold the data; and

a boost circuit to boost a gating signal on the nonvolatile fuse to enable the nonvolatile fuse to transfer the data.

69. The wireless device of claim 68 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the nonvolatile fuse comprises a flash cell comprising a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being boosted from a voltage supply in the range of 1.65 volts to 2.22 volts, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter;

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell in response to the boosting signal.

70. A wireless device comprising:

a display;

a processor; and

a flash memory device comprising a fuse circuit, the fuse circuit comprising:

a volatile latch circuit to latch data;

a flash cell to hold the data; and

a boost circuit to boost a gating signal on the flash cell to enable the flash cell to transfer the data.

71. The wireless device of claim 70 wherein:

the wireless device further comprises an antenna;

the flash memory device was formed in an integrated circuit and further

comprises:

an array of memory cells;

a decoder coupled to the array to decode address signals to select a memory cell in the array; and

a redundancy circuit coupled to the array to provide redundant memory elements for the array, the redundancy circuit including the fuse circuit;

the flash cell comprises a gate coupled to receive the gating signal, a drain, and a source coupled to ground, the boosted gating signal being sufficient to turn on the flash cell if the flash cell is in an erased state and the boosted gating signal being insufficient to turn on the flash cell if the flash cell is in a programmed state;

the volatile latch comprises an output of a first inverter coupled to an input of a second inverter and the drain of the flash cell and an output of the second inverter coupled to an input of the first inverter; and

the boost circuit comprises a capacitor coupled between the gate of the flash cell and a boosting signal to boost the gating signal on the gate of the flash cell from a voltage supply in the range of 1.65 volts to 2.22 volts in response to the boosting signal.